PWR SOC '14

Integrated Power Conversion and Power Management

next generation technology for emerging business opportunities

new technologies new applications new markets

Tuesday, October 7th, 2014 – Session 4: Magnetics

Galvanic Isolating Power Supplies – From PCB to Chip & from Analogue to Digital

Matthias Radecker, Yujia Yang, Torsten Reich, René Buhl, Hans-Joachim Quenzer, Shan-Shan Gu-Stoppel

Fraunhofer IZM Fraunhofer IIS Fraunhofer ISIT

Outline

- Galvanic Isolation versus Miniaturization
- Size Reduction at PCB
- Integration on Silicon versus Passive Process
- Piezo Transformer: Discrete and on Silicon
- GaN on Silicon
- Interleaved Driving for Matching Modules
- Digital Driving for Flexible Programming
- Sequence Based Control & Transient Control
- Conclusion

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Galvanic Isolation versus Miniaturization

Isolation by discrete components

- Magnetic transformer: Winding Isolation and Pin Distance on PCB large (8 mm creepage distance)
- Capacitor: Large Coupling Capacitance, maximum power limited, 8 mm creepage distance
- Piezoelectric transformer: Size must allow for 8 mm creepage distance, pin distance on PCB large
- High power density with galvanic isolation is only possible with integrated technology

Galvanic Isolation & Miniaturization

Isolation by passive technology: **114 W/cm³**

- Integrated magnetic transformer: Isolation by material, no air creepage distance, V = 10,5 cm³
- \+ multilevel input stage -> reduce blocking voltage
- \+ low Q -> unregulated
- \+ high frequency

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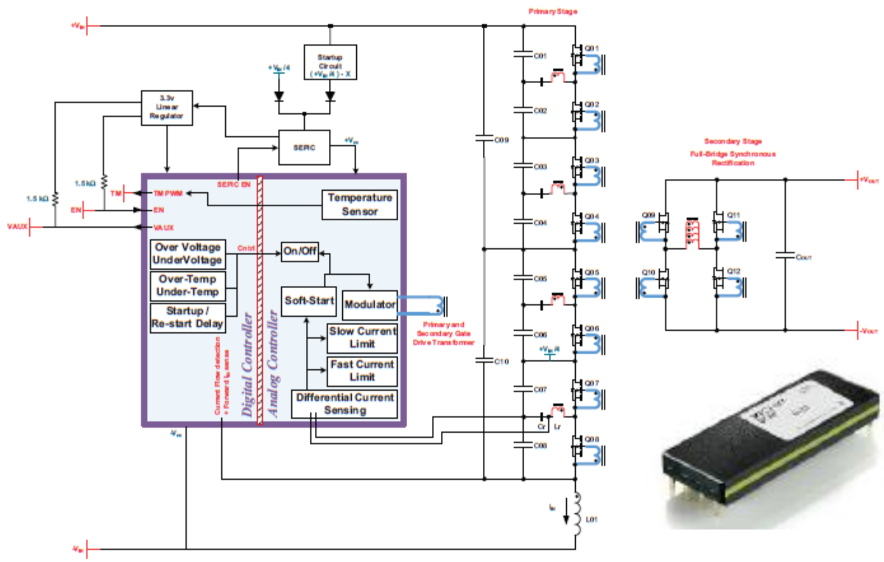
- = Miniaturization

Source: VICOR **BCM® Bus Converter**
BCM380y475x1K2A30



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Size Reduction at PCB

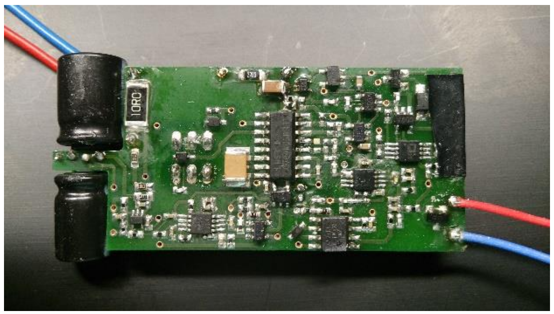
LED Off-Line 12 Watts: 0,7 W/cm³ - Transformer Size:

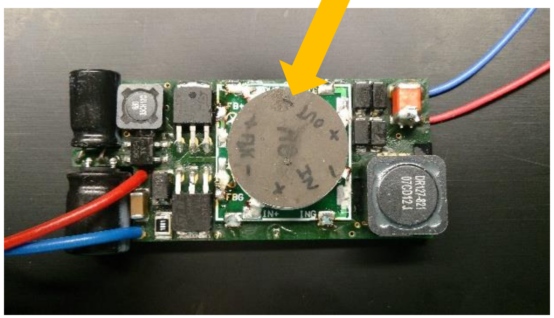
- PCB: 78x34x15 mm³=39,78 cm³
  (opt.) 24,3 cm³ (low cost)164 %
- PCB: 60x27x12 mm³=19,44 cm³
  (optimized) 80 %
- PCB: 60x7x10,5 mm³=17,01 cm³
  (optimized) 70 %

Flyback H=8,5 mm
2,04 cm³ 100 %

Piezo Radial H=5,2 mm
1,47 cm³ 72 %

Piezo Quad. H=3,75mm
0,85 cm³ 42 %

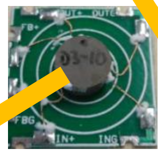


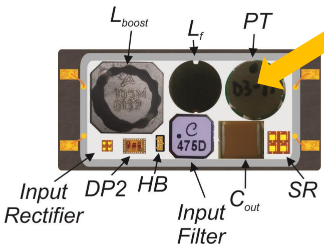


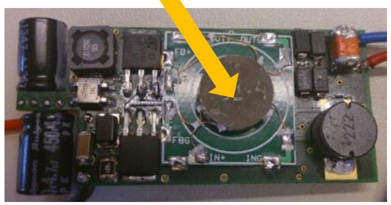
Size Reduction at PCB depends mainly on height of transformer

Size Reduction at PCB

Off-Line Power Supply 4 Watts: **0,68 W/cm³** - Frequency:

- PT Radial 200 kHz  D=14 mm; H=4 mm (V=0,62 cm³)
- PT Radial 280 kHz  D=10 mm; H=3.5 mm (V=0,28 cm³)





Multi-leaded Power package (e.g. SDIP-38L = 5,9 cm³)	PCB: 40x25x8 mm³ = 8,0 cm³	RAC04-C (RECOM) = 10,7 cm³
74%	100%	134 %

Power package for small height converter components suitable

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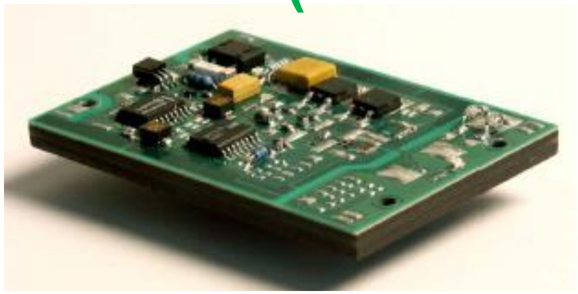
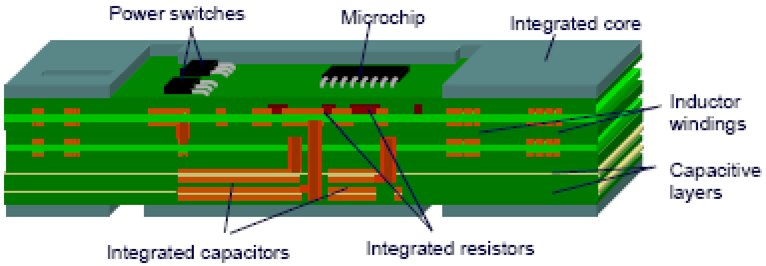
Integration on Silicon versus Passive Process

„emPIC“ (embedded passives integrated circuit)

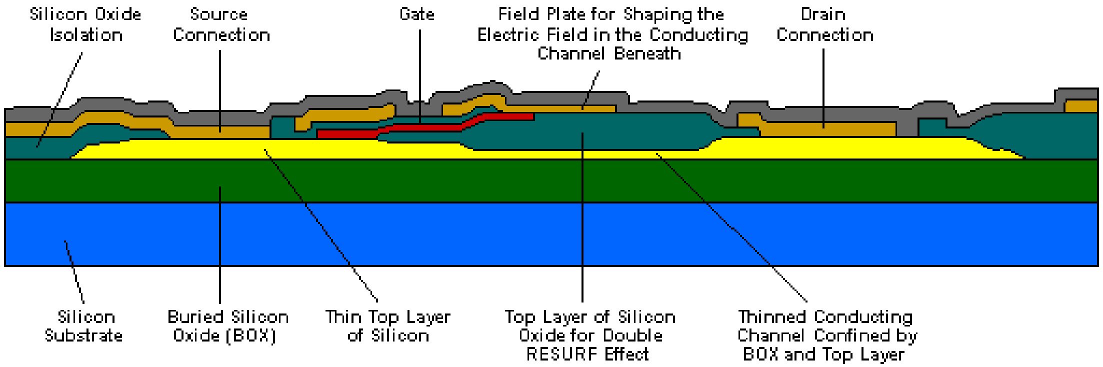




Source: Waffenschmidt, E.; Ferreira, J.A.; "Embedded passives integrated circuits for power converters "; PESC 02. 2002 IEEE 33rd Annual, Volume: 1 , 23-27 June 2002; Pages:12 - 17 vol.1.

Ballast-on-a-chip: Di-electric Isolation

EZ-HV™, Philips Semiconductors (SOI-technology)



Silicon Technology and Passive Technology with L in range of µH not compatible

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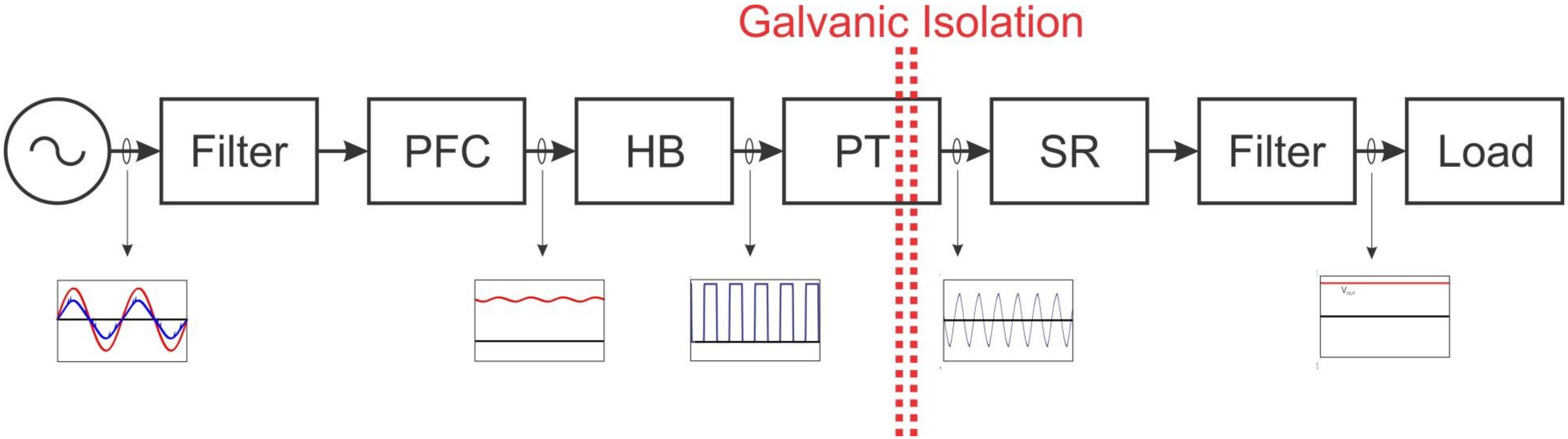
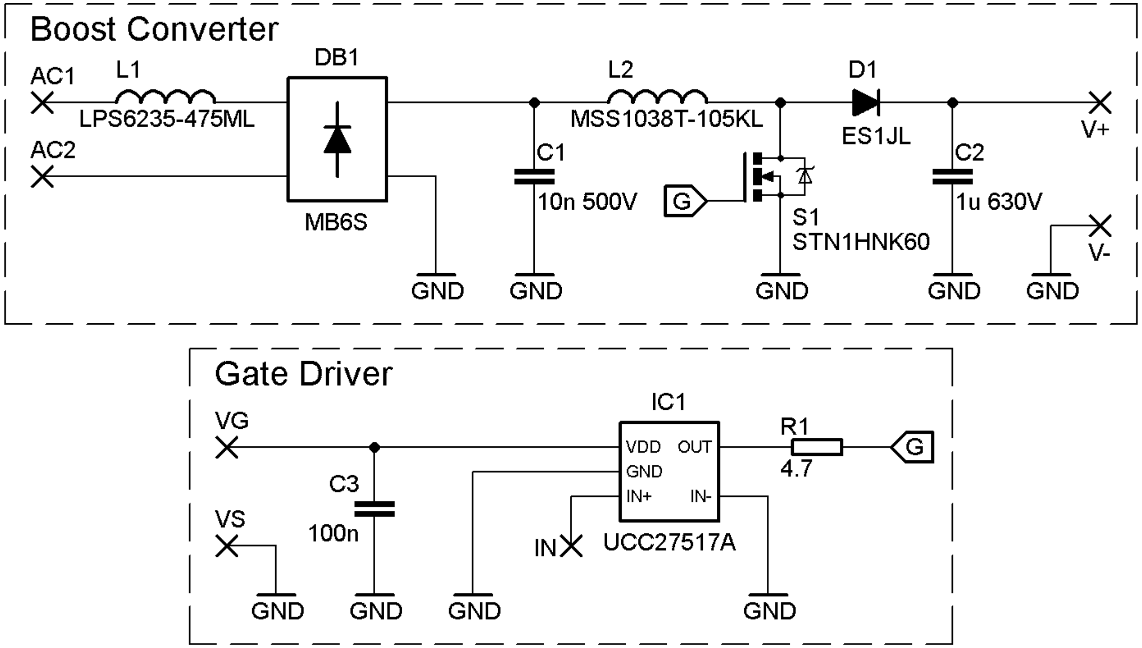
Topology Off-Line Piezo Power Supply

IF + Boost Converter (PFC) + Serial Inductor HB + Piezo Transformer + Syncronous Rectifier FB + OF



Topology Off-Line Piezo Power Supply

Input Filter + Boost Converter (PFC)



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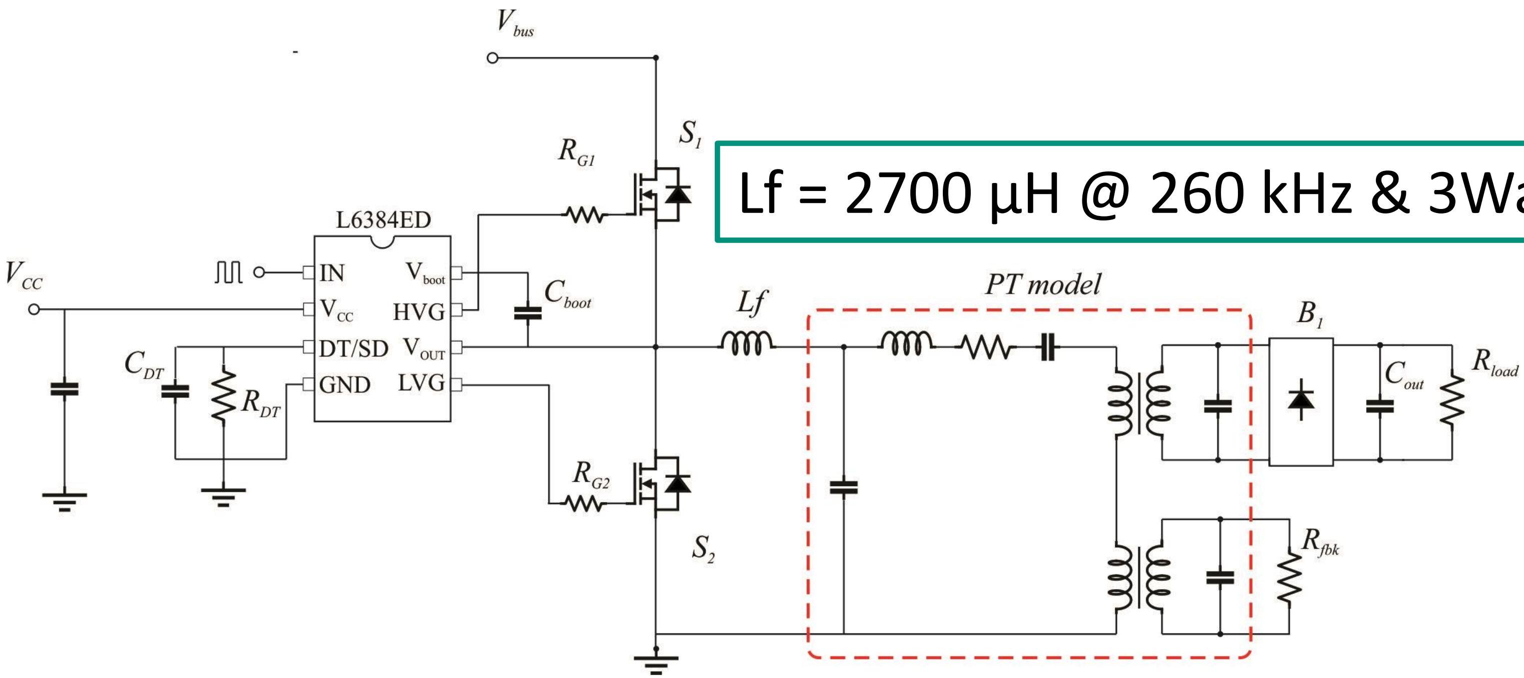
Topology Off-Line Piezo Power Supply

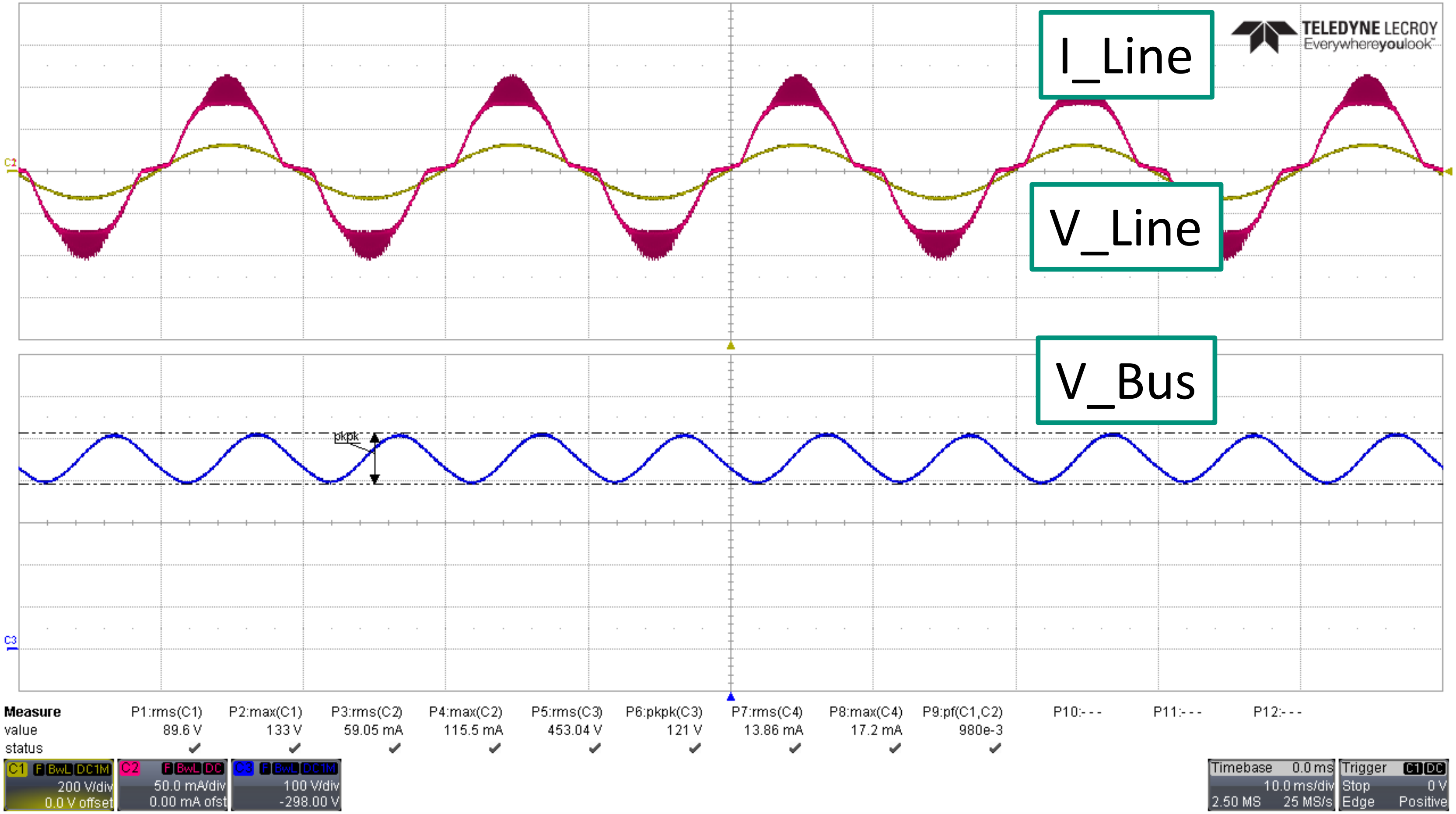
Serial Inductor HB + Piezo Transformer + Synchronous Rectifier FB + Output Filter



Lf = 2700 µH @ 260 kHz & 3Watts

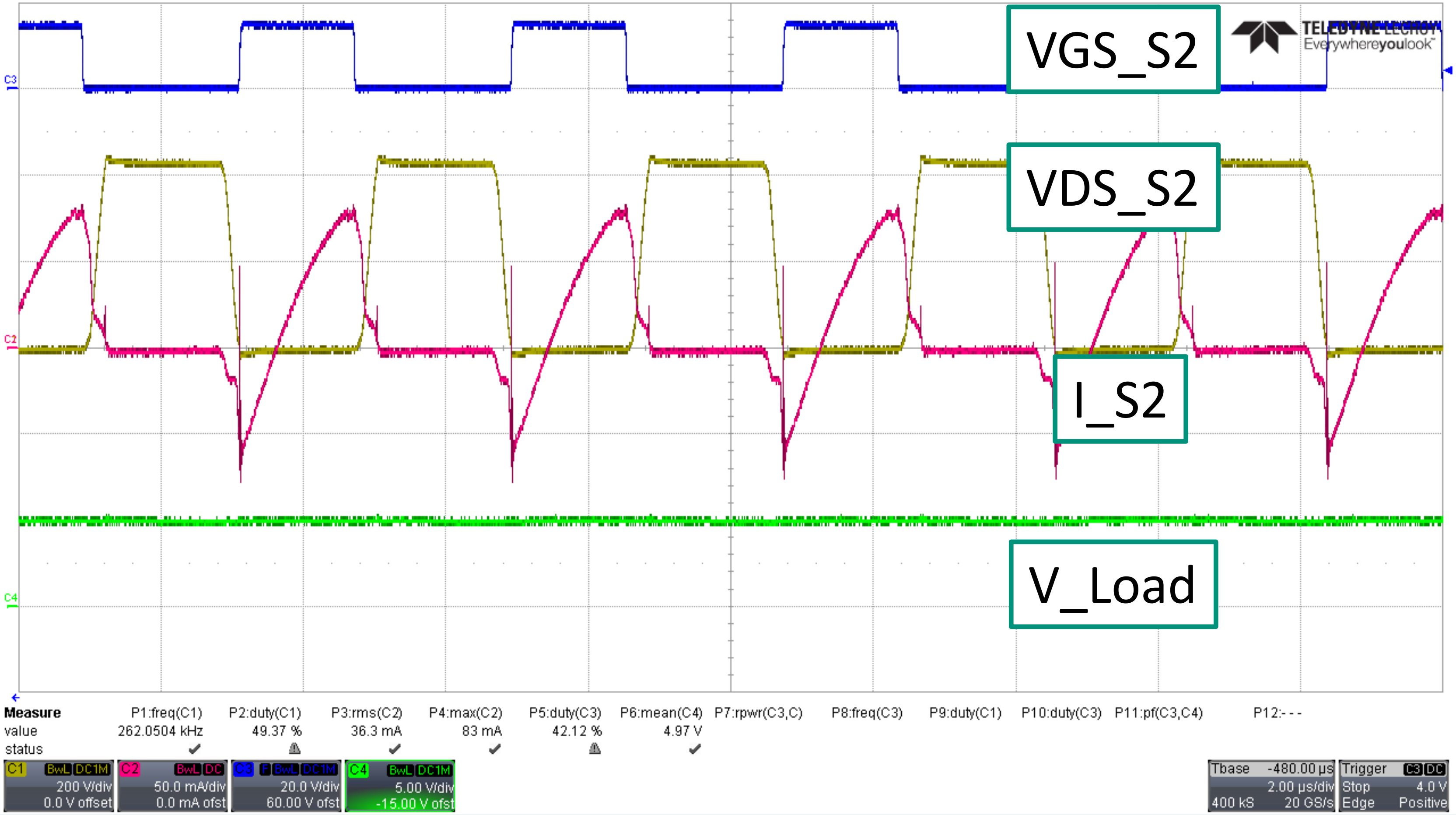
Experimental Results 3 Watts

Input Filter + Boost Converter (PFC) V_{IN} = 90V_{rms}



Experimental Results 3 Watts

SIHB + PT + Rectifier + Output Filter: V_{BUS} = 450V



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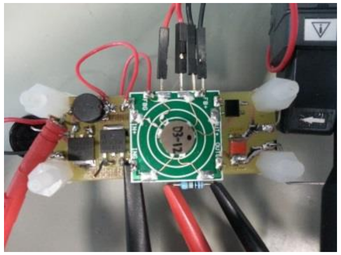
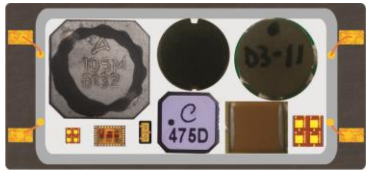
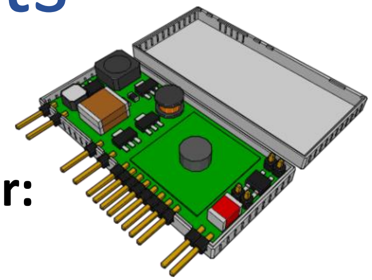
Experimental Results 3 Watts



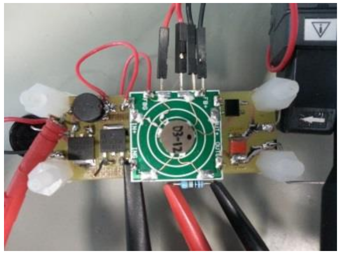


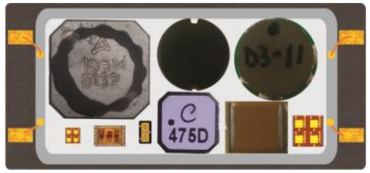
Or:



Parameter	Value
Switching Frequency	261.86 kHz
Average output voltage	4.947 V
Average output power	3.138 W
Half-Bridge Lf rms current	55 mA
Ambient Temperature	28 °C
PT maximum temperature	62 °C
Lf maximum temperature	46 °C
S1, S2 maximum temperature	38 °C

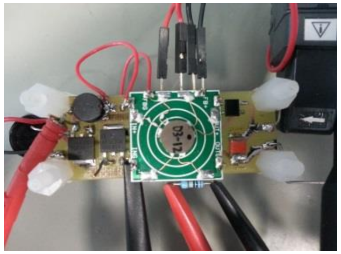
Goal: All Components **Integrated on Silicon**

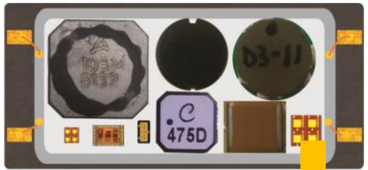


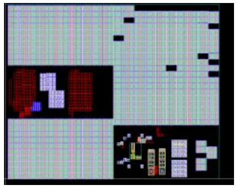


Simple and Reliable Packaging !

Integrated Synchronous Rectifier



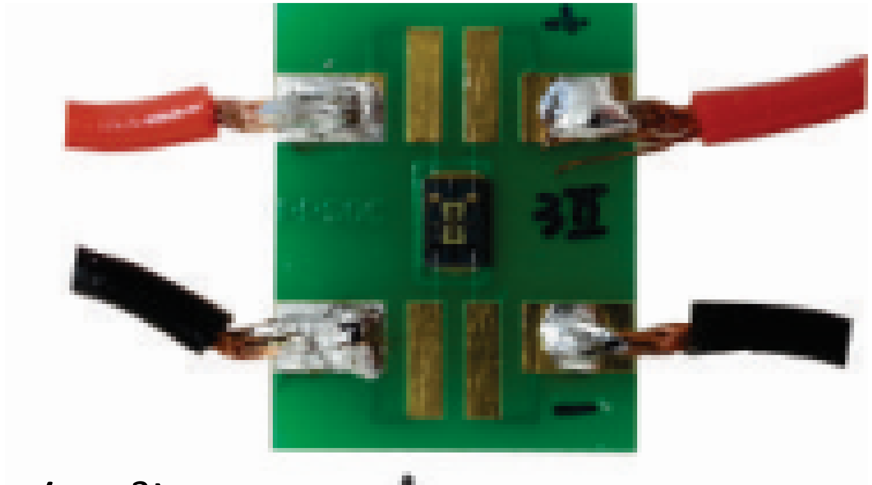




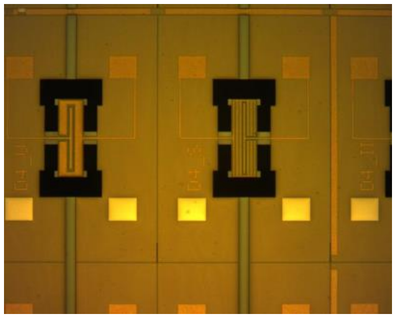
$3.5\ mm^2$ @ $P_{out\ max} = 5$ Watts
(CMOS)

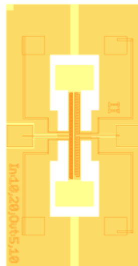
Integrated Piezo Transformer

Discrete Device
(PZT Power Density = 20 … 40 W/cm³)



Single Integrated Device

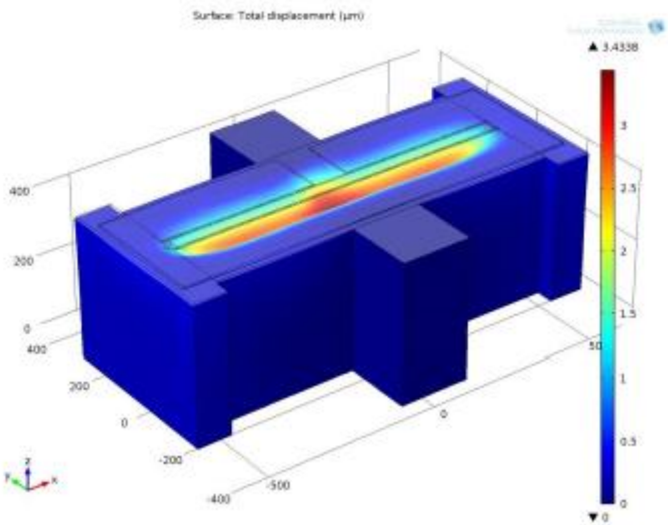




- How to integrate a PT on Silicon?

Integrated Array
(Goal: PZT Power Density = 20000 … 40000 W/cm³)

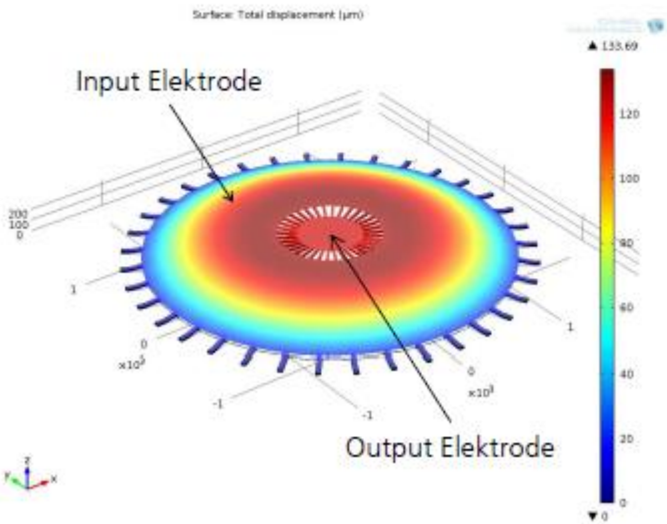
Integrated Piezo Transformer



- Thickness PZT: Tp = 4 µm
- Thickness Silicon: Tsi = 400 µm
- Input Voltage = 100 V
- Output Voltage = 11.3 V
- Strain Output Electrode-Membrane:
  - maximum planar: 0.14 µm
  - maximum vertical: 2.5 µm
  - average planar: 0.08 µm
  - average vertical: 1.6 µm
- average stress: 2.89 * 10^8 Pa

- Dumbbell-shaped Hollow-Out U Device

Integrated Piezo Transformer



- Thickness PZT: Tp = 2 µm
- Thickness Silicon: Tsi = 20 µm
- Input Voltage = 100 V
- Output Voltage = 22.3 V
- Strain Output Electrode-Membrane:
  - maximum planar: 1.1 µm
  - maximum vertical: 1.2 µm
  - average planar: 0.77 µm
  - average vertical: 1.0 µm
- average stress: 6.23 * 10^8 Pa

- Double Ring Device

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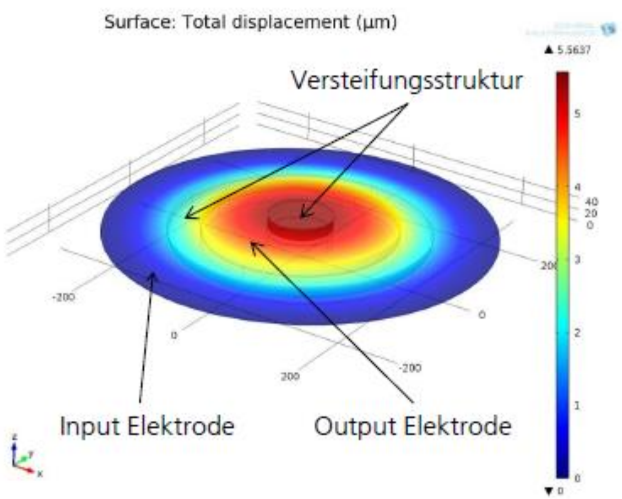
Integrated Piezo Transformer



- Thickness PZT: Tp = 2 µm
- Thickness Silicon: Tsi = 20 µm
- Input Voltage = 100 V
- Output Voltage = 16.8 V
- Strain Output Electrode-Membrane:
  - maximum planar: 0.5 µm
  - maximum vertical: 1.9 µm
  - average planar: 0.3 µm
  - average vertical: 1.1 µm
- average stress: 5.06 * 10^8 Pa

- Drum-shaped Device

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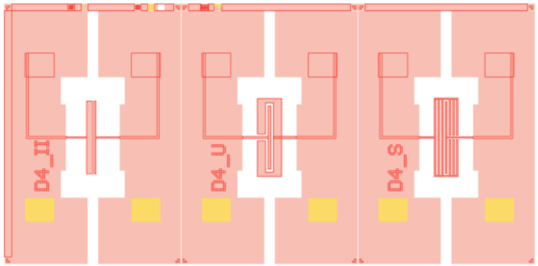
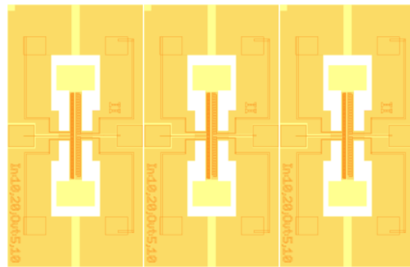
Integrated Piezo Transformer

	Discrete PT	Massive U Design	Hollow-Out U Design	Double –R. Design	Drum Design
Displacement vertical (µm)	6e-4	0,87e-2	1,6	1	1,1
Average Stress (Pa)	1,08e8	2.29e7	2,89e8	6,23e8	5,06e8
Input Voltage (V)	100	100	100	100	100
Output Voltage (V)	29	1,45	11,3	22,3	16,8

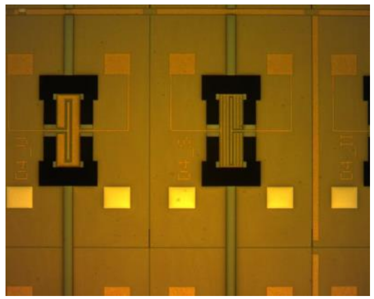
- Decision: Hollow-Out U Design

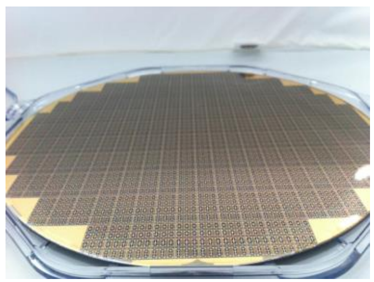
Integrated Piezo Transformer





- Top Layer (Au) with Bottom Layer (Pt) has large conduction resistance and capacitive shorts

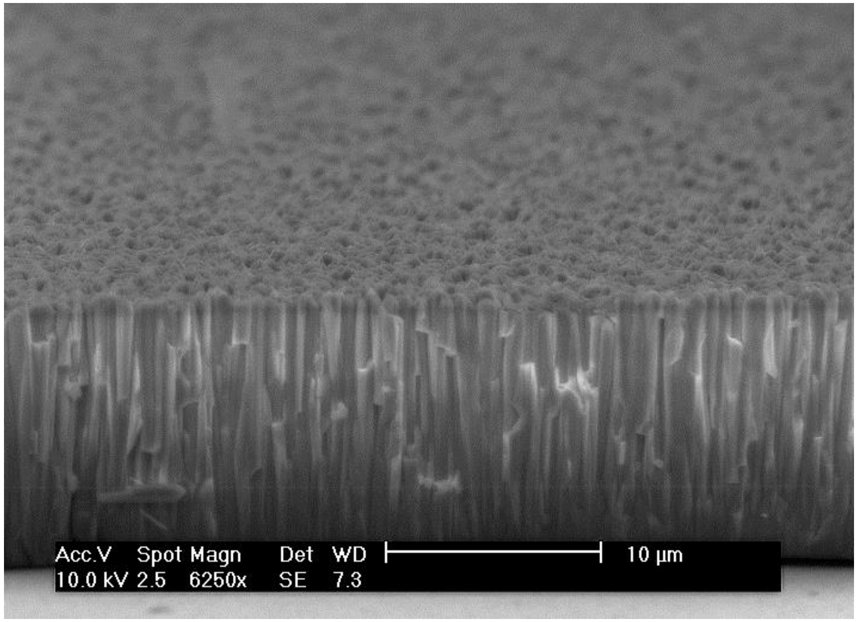




- Interdigital Structure for only Top Layer (Au) has minimum conduction resistance and small capacitances

Sputtering of PZT

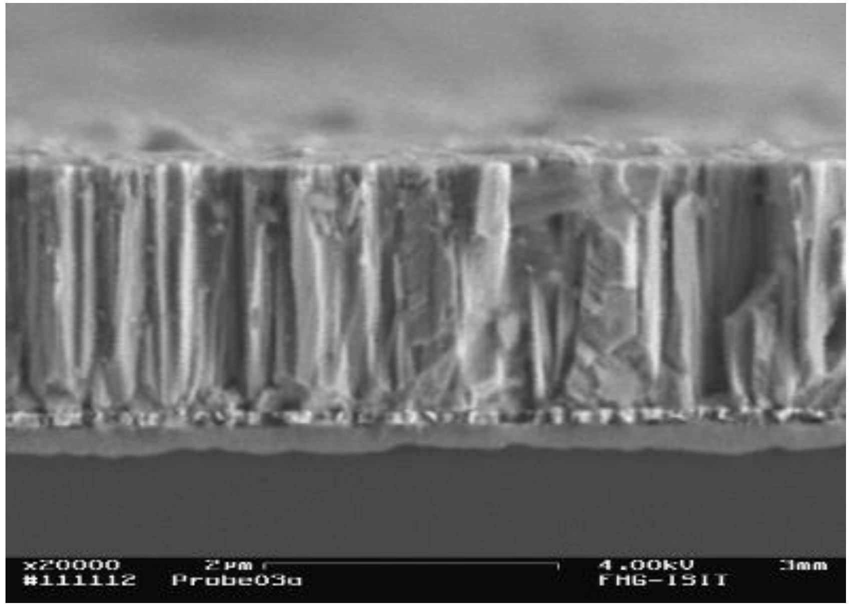
Choice of Sputtering Process: High Power Density achieved by unique crystal structure



PZT-Schicht auf Si durch

PZT on Si through hollow cathode sputtering 13,3 µm thickness,

(100 µm thickness possible)



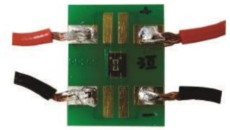
Magnetron Sputtering of PZT

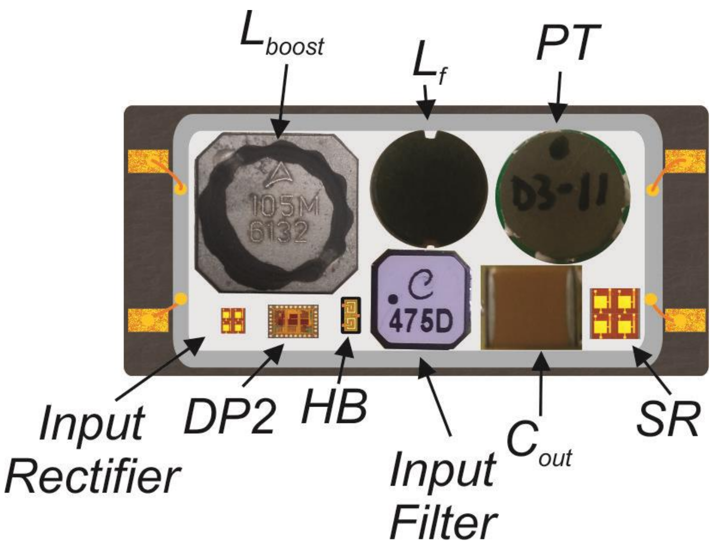
- 8" Siliziumwafer
- hot sputtering process T =550°C
- metallic targets
- Sputtering rate 100 nm/min

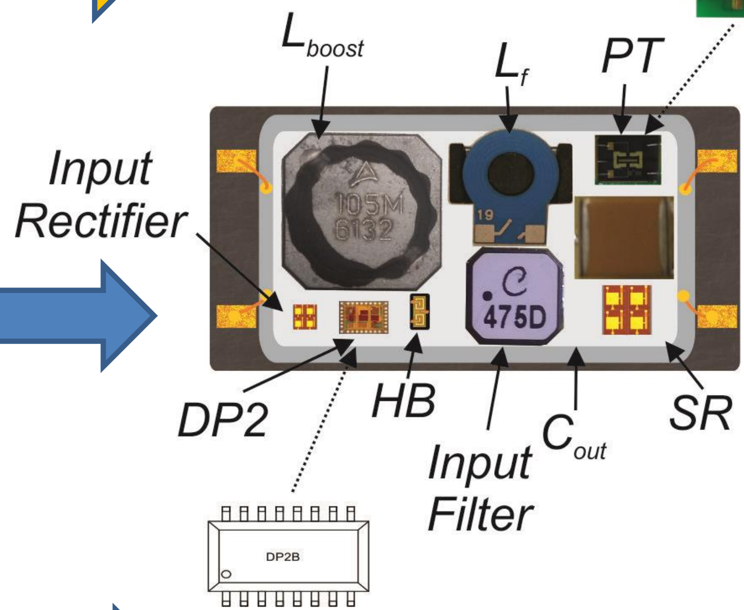
Integrated Piezo Transformer Application

Conventional Inductor → LTCC Inductor or Integrated

Discrete PT → Integrated PT







Conventional Analog Driver ICs → Digital Driver Plattform

Si Mosfets for HB → GaN Mosfets for HB

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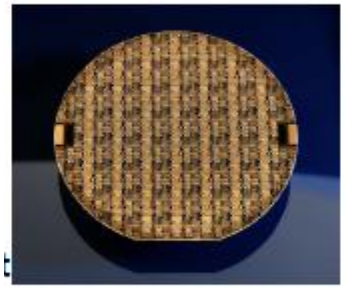
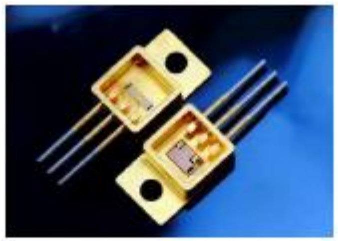
GaN Integrated on Silicon

- GaN has high blocking voltage
- High temperature capability
- Small On-Resistance
- High swiching frequencies
- GaN on large and cheap silicon subtrates
- Arrays feasible (Half-Bridge)

GaN: E_c = 3,3 MV/cm
Si: E_c = 0,3 MV/cm





But: For Voltages over 100 V no benefit compered to Silicon (e.g. Coolmos)

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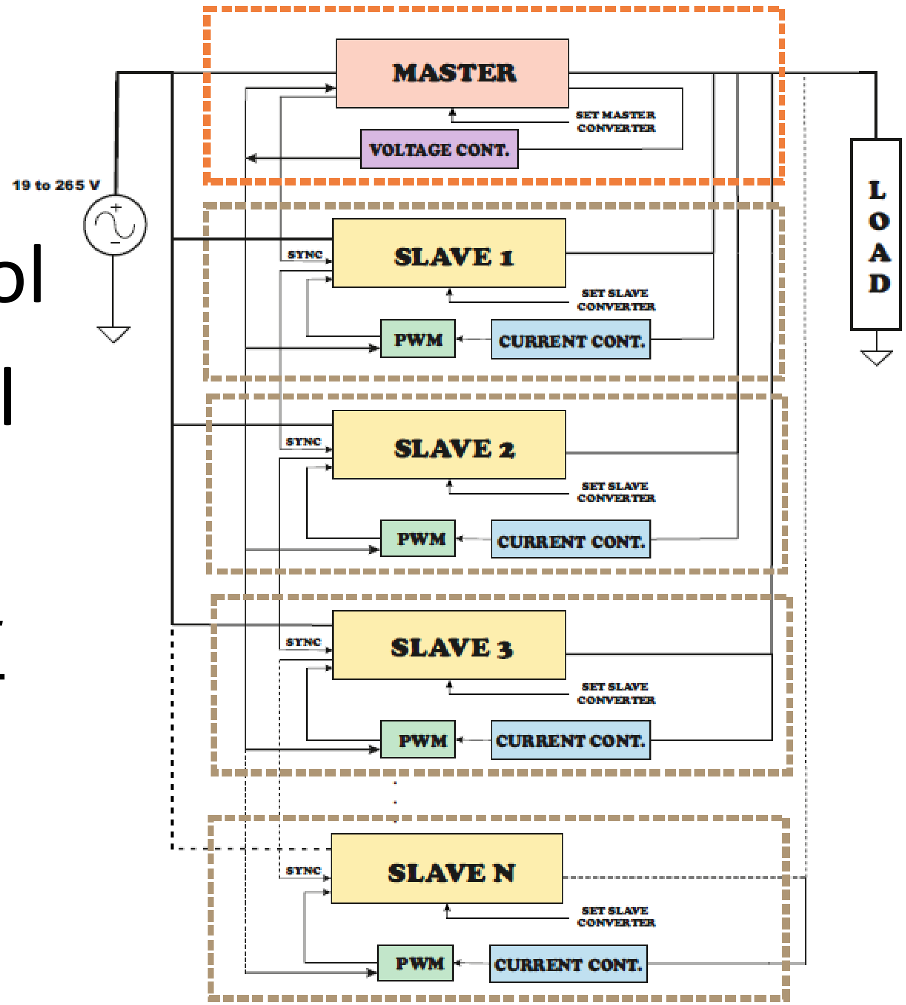
Interleaved Driving for Matching Modules

- Modules operate on demand
- Master: Voltage Control
- Slaves: Current Control



- Phase Shifting: $\varphi = \frac{2\pi}{n}$
- Reduces Output Filter
- Reduces Input filter

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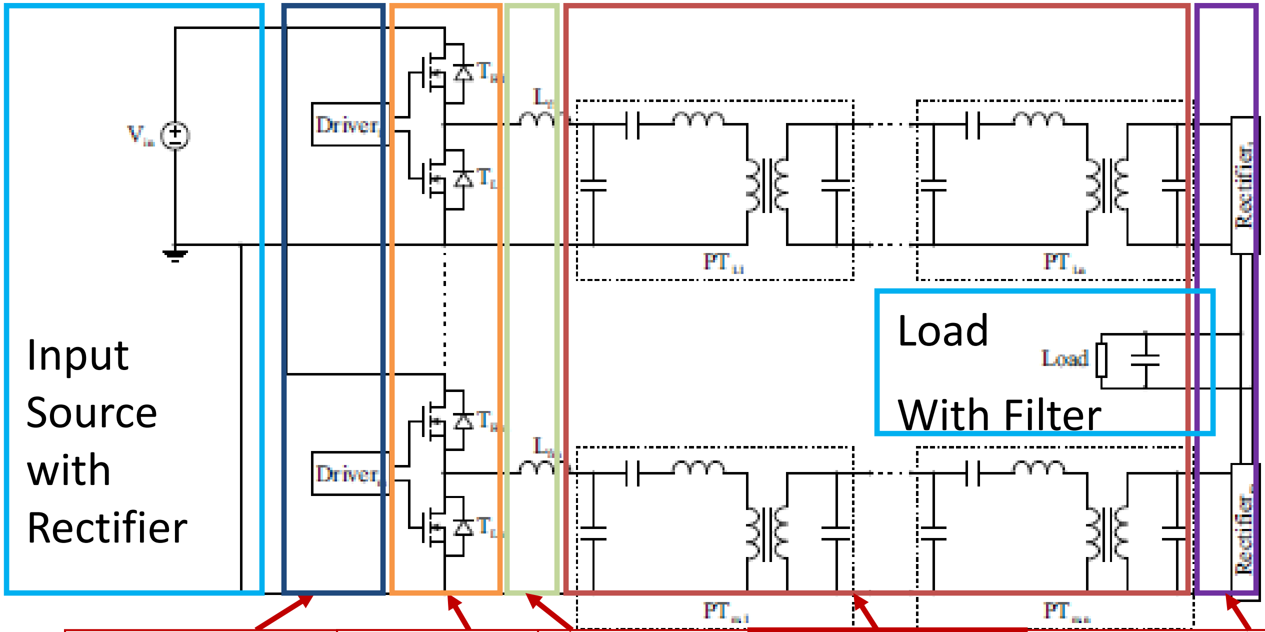
Granular Structure for Matching Modules



Control Chipset: Nano-DSP, Low-Side- and High-Side Driver	GaN on Si or Si Half-Bridge Multi-level Chipset	Inte-grated Induc-tors **(nH -> MHz !)**	Modul of integrated Micro-Piezo-Trafo-Strings (PZT-MEMS)	Integrated Synchronous Rectifier Chip

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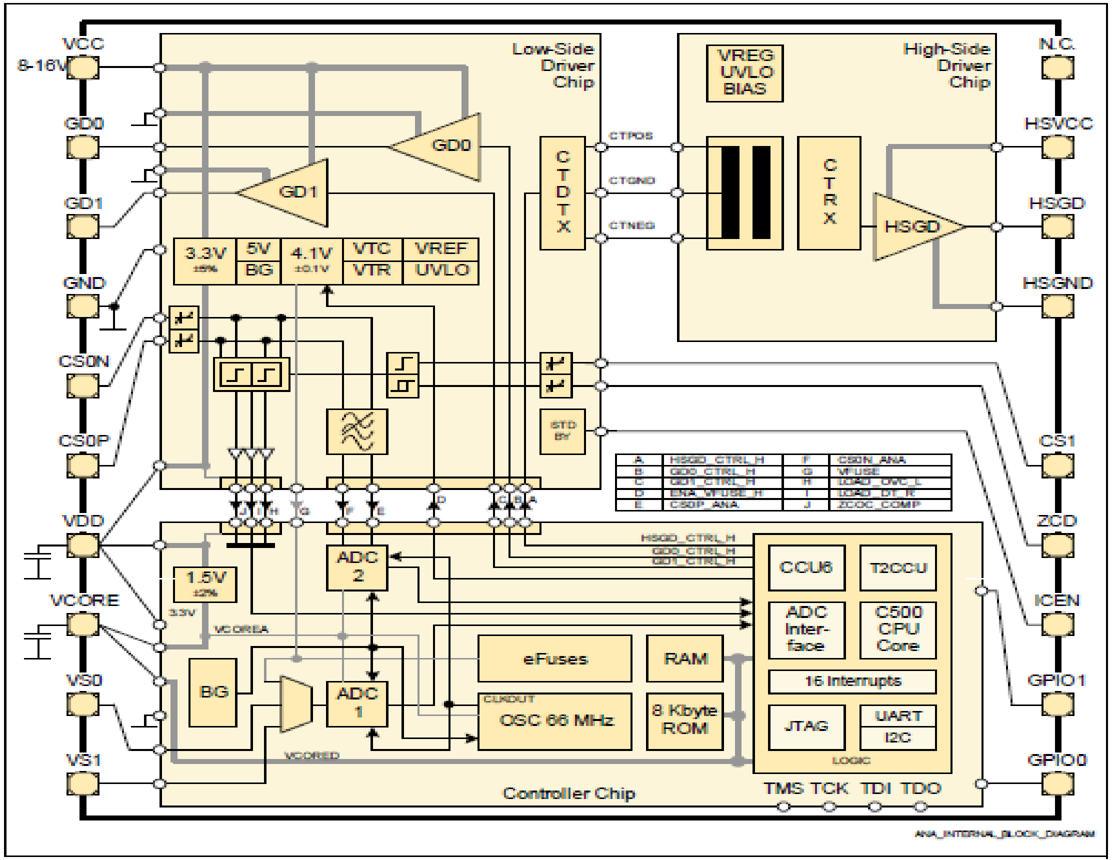
Digital Driving for Flexible Programming

- Chip by Chip
- Nano-DSP for Digital Control
- Low-Side Driver
- High-Side Driver up to 1 MHz
- Programmable Pins
- Interleaving by GPIO



Source: DP2 of Infineon Technologies AG

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Sequence Based Control and Transient Control

- Sequence Based Control (SBC) means extended sliding mode control considering linear and saturated areas
- SBC can improve transient behaviour significantly and avoid instablility of PWM converters
- Modular topology with interleaved cells controllable by SBC
- SBC requires Digital Control (DSP)

- Transient Control (TC) will control switching slopes at power switches for improving EMI suppression and reducing filter expense
- Transient Control (e.g. dV/dt of Drain-Source Voltage) will improve interleaving ripple reduction (avoid spikes)
- TC requires Digital Control (DSP)

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Conclusion

- Power density of galvanic isolating off-line supplies for several Watts is not satisfying today
- Magnetic transformer technology is not compatible yet with silicon integration, only at > 100 MHz
- Piezoelectric transformers have larger power density than magnetics and can be integrated on silicon
- High efficient power switches as GaN transistors can be integrated on silicon to reduce switching losses, only with granular structure for V_{BR} < 100 V
- Interleaved driving reduces filter expense
- Integrated arrays of piezo transformers improve matching
- Digital driving provides functional flexibility and enable appropriate control methods (SBC, TC)

Thank you !

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